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1. A method for programmably allocating system resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system comprising the steps of:
 - determining the number and type of transactions anticipated at a port,
 - determining the number and type of devices being serviced via the port,
 - setting criteria for transactions at the port with respect to the number and type of transactions and devices,
 - assigning the system resources to the port with respect to the criteria.
 2. The method as defined in claim 1 further comprising the steps of:
 - providing at least one control register for each port, wherein the control register includes a plurality of programmable fields.
 3. The method as defined in claim 2 further comprising the steps of configuring the control register fields to contain a number of direct memory access engines available at a port to support a transaction, a number of cache lines for requested data, and a number representing priorities among the anticipated transactions.
 4. The method as defined in claim 1 further comprising the step of preparing for hot swapping an assembly, wherein the preparing for hot swapping comprises, with respect to the assembly being replaced, copying the assembly's state, the state of its associated memory systems, its status and control registers, and the contents of its cache and memory systems.
 5. The method as defined in claim 4 wherein the copying comprises the steps of:
 - flushing the data in the local cache and local memory to storage not affected by the hot swapping,
 - invalidating data in cache,
 - setting a flush indicator in the port's cache status and control register,
 - flushing directory data to non-affected storage,

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7 finding and stopping any new transactions,
8 completing any transactions already started or pending,
9 flushing the translation look-aside buffers,
10 invalidating the contents of the translation look-aside buffers, and
11 updating the system directory.

1 6. A system for allocating system resources to accommodate I/O transactions at I/O
2 ports of a multiprocessor computer system comprising:
3 the number and type of transactions anticipated at a port,
4 number and type of devices being serviced via the port,
5 criteria for operations at the port with respect to the number and type of transac-
6 tions and devices,
7 means for assigning the system resources to the port with respect to the criteria.

1 7. The system as defined in claim 6 further comprising:
2 at least one control register for each port, wherein the control register includes a
3 plurality of programmable fields.

1 8. The system as defined in claim 7 wherein the control register fields include a
2 number of direct memory access engines available at a port to support a transaction, a
3 number of cache lines for requested data, and a number representing priorities among the
4 anticipated transactions.

1 9. The method as defined in claim 6 further comprising:
2 means for hot swapping of an assembly, including means for copying the assem-
3 bly's state, the state of its associated memory systems, its status and control registers, and
4 the contents of its cache and memory systems.

1 10. The system as defined in claim 9 wherein the means for copying comprises:
2 means for flushing the data in the local cache and local memory to storage not af-
3 fected by the hot swapping,

- 4 means for flushing, modifying and invalidating unmodified data in cache,
5 means for setting a flush indicator in the port's cache status and control register,
6 means for flushing directory data to non-affected storage,
7 means for finding and stopping any new transactions,
8 means for completing any transactions already started or pending,
9 means for flushing the translation look-aside buffers,
10 means for invalidating the contents of the translation look-aside buffers, and
11 means for updating the directory.
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